NOTE: Click once on shaded fields to type data. To check boxes, right click at box, click “Properties”, and click “Checked” under Default Values.

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<th>DEPARTMENT/PROGRAM</th>
<th>Electrical and Computer Engineering</th>
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<tr>
<td>COURSE PREFIX/NUMBER</td>
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<td>INSTRUCTOR (NAME/RANK)</td>
<td>Winser E. Alexander, Professor</td>
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<td>Graduate Faculty Status</td>
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CATALOG DESCRIPTION (limit to 80 words): Design of parallel algorithms and special purpose computer architectures for digital signal and image processing applications with emphasis on high-speed communications and computational engineering. Design of high performance digital systems at different levels of abstraction including the functional level, the transaction level and the register transfer level.

RECOMMENDED BY:

Department Head/Director of Graduate Programs

ENDORSED BY:

Chair, College Graduate Studies Committee

APPROVED:

Dean of the Graduate School
This course is being revised to update it because of advances in the design of special purpose computer systems and to change the prerequisites to better match the background that students need to study the subject. The addition of material on the design of digital systems at the transaction level and the functional level replaces the discussion of fundamental digital signal processing algorithms. The proposed solution is to change the digital signal processing prerequisite from the upper level undergraduate course, ECE 421, to the graduate level digital signal processing course, ECE 713 and to change the system design prerequisite from ECE 406 to a co-requisite for ECE 520. After these changes, the fundamental digital signal processing algorithms will not be covered in ECE 747 and the incoming graduate students can cover the basics of system hardware design in the first part of ECE 520.

The previous course material emphasized the design of digital systems at the register transfer level only. The revised course will study the design of digital system beginning at the functional level with refinement of the design to the transaction level and finally to the register transfer level.

PREVIOUS COURSE DESCRIPTION

Design of parallel algorithms and special purpose architectures for digital signal and image processing applications with emphasis on high-speed communications and computational engineering. Mapping digital signal and image processing algorithms to pipeline arrays, systolic arrays, wave-front arrays and other parallel architectures. Register transfer level design of application-specific and special-purpose digital processing systems.

NEW COURSE DESCRIPTION

See cover page. The new description better reflects the higher level and system emphasis of the updated course.

ENROLLMENT LAST 5 YEARS

This course has been taught during spring semester for the last several years. Enrollment is given in the following Table 1.

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<tr>
<th>Year (Spring)</th>
<th>2001</th>
<th>2002</th>
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<th>2004</th>
<th>2005</th>
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<td>15</td>
<td>21</td>
<td>36</td>
<td>15</td>
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</table>

Table 1. Enrollment in ECE 747 for the last 5 years.

Spring semester 2005 can be considered as a transition semester. The syllabus for spring 2005 was essentially the proposed syllabus for spring 2006 with minor variations.

Learning Objectives

See syllabus
ECE 747 - DIGITAL SIGNAL PROCESSING ARCHITECTURE  
Spring 2006  
Proposed Course Syllabus

Class Schedule - days: TH

Instructor: Dr. Winser E. Alexander  
Professor of ECE  
Office – 1408 Flex Laboratories  
Office Phone - (919) 515-5190  
email - winser@ncsu.edu

PREREQUISITES
The prerequisites for this course are as follows:
1. A graduate level course in digital signal processing ECE 713.
2. Basic knowledge of computer architecture and digital system design including knowledge of the use of Verilog to describe hardware systems ECE 520.

COURSE DESCRIPTION
ECE 747 - DSP Architecture. Preq: ECE 713, Coreq: ECE 520. Spring. Design of parallel algorithms and special purpose computer architectures for digital signal and image processing applications with emphasis on high-speed communications and computational engineering. The design of high performance digital systems at different levels of abstraction including the functional level, the transaction level and the register transfer level.

The following subjects are covered:
1. Special purpose and application specific architectures for digital signal processing – 5 lectures
2. Computational Structures for DSP Algorithm – 5 lectures
3. Exam 1 – 1 lecture
4. System and Software Design Issues – 5 lectures
5. Modeling and Simulation for Computer Systems Design – 5 lectures
6. Exam 2 – 1 lecture
7. Case Studies for DSP Systems Design – 6 lectures

GOALS AND EXPECTED OUTCOMES
This course is oriented toward the design, modeling and simulation of special purpose and application specific computing systems for digital signal processing, image processing and communications. Upon completion of the course, the students will be able to:
1. state the relationship of algorithms to performance of hardware systems,
2. develop algorithms with low data communication requirements as well as minimum computational complexity,
3. map algorithms to special purpose hardware systems,
4. design special purpose and application specific digital systems at different levels of abstraction including the functional level, the transaction level and the register transfer level, and
5. evaluate the parameters related to expected performance for application specific and special purpose digital systems designs.
6. design of an actual digital system at different levels of abstraction (course project).

The course emphasizes the design of special purpose and application specific computer systems for applications that require high performance such as digital signal processing, communications and image processing.

TEXT AND REFERENCES
On line course notes by the Instructor will replace the primary text for this course. In addition, online tutorials and manuals for SystemC at www.systemc.org will be used as appropriate. Additional references include:
COURSE REQUIREMENTS
The course requirements are:
1. two in class exams during the semester,
2. a final exam,
3. homework assignments including some that require writing computer programs to model and simulate hardware designs.
4. a class project involving the design of a digital system for an application in communications of image processing.

The computer work will involve algorithm development, system design and simulation. We will discuss the use of Matlab, C++, Verilog and SystemC for simulations, modeling and performance evaluations in the class. The University computing system will be used for all required computer simulations, etc. Other classes such as ECE 406 and ECE 520 use Verilog and lockers for these courses have helpful hints on its use.

A PC or any workstation may be used instead of the Eos computing system with appropriate software as follows:
1. Matlab (The student version of Matlab with the Signal Processing Tool Box is the minimum acceptable level)
3. C++ software that is compatible with SystemC.

GRADING POLICY
The plus-minus grading systems will be used for this course. Grades will be based upon:
1. the two semester exams (20% each for a total of 40%),
2. a final exam (25%),
3. homework and computer assignments (15%).
4. a class project (20%)

STATEMENT ON LATE ASSIGNMENTS
All assignments must be turned in at the beginning of class on the date they are due. Students who believe they have valid excuses to miss exams must comply with University Attendance Regulations, see http://www.ncsu.edu/provost/academic_policies/attend/reg.htm

COURSE LOCKER
The Wolf Ware course locker for this course will be used to provide course notes, to additional information on the course, to make homework assignments, to provide examples, etc. You can obtain access to the course locker by using a Web browser such as Netscape or Explorer. The URL for the locker is http://courses.ncsu.edu/ece747/

STUDENTS WITH DISABILITIES
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. http://www.ncsu.edu/dss/.

For more information on NC State's policy on working with students with disabilities, please see http://www.ncsu.edu/provost/hat/current/appendix/appendix_k.html

ACADEMIC INTEGRITY
All the provisions of the code of student conduct apply to this course as appropriate. See http://www2.ncsu.edu/prr/student_services/student_conduct/POL445.00.1.htm
Class Schedule - days: TH, time: 4:05 – 5:20

Instructor: Dr. Winser E. Alexander
Professor of ECE
Office - 311 Daniels Hall
Office Phone - (919) 515-5190
e-mail - winser@ncsu.edu

PREREQUISITES
The prerequisites for this course are as follows:
1. An introductory course in digital signal processing ECE 421.
2. Basic knowledge of computer architecture and digital system design including
   knowledge of the use of Verilog to describe hardware systems ECE 406.

COURSE DESCRIPTION
algorithms and special purpose computer architectures for digital signal processing, image
processing and communication systems with emphasis on high throughput and accuracy.
Mapping digital signal and image processing algorithms to parallel and pipeline
architectures. Register transfer level design of application-specific and special-purpose digital
systems.

The following subjects are covered:
1. Special purpose and application specific architectures for digital signal processing – 3
   lectures
3. Exam 1 – 1 lecture
4. Computational Structures for DSP Algorithm – 5 lectures
5. System and Software Design Issues – 2 lectures
6. Modeling and Simulation for Computer Systems Design - 3 lectures
7. Exam 2 – 1 lecture
8. Multirate Signal Processing – 3 lectures
9. Case Studies for DSP Systems Design – 3 lectures

GOALS AND EXPECTED OUTCOMES
This course is oriented toward the design and simulation of special purpose and application
specific computing systems for digital signal processing, image processing and
communications. Students will learn:
1. the relationship of algorithms to performance of hardware systems,
2. procedures for the development of algorithms with low data communication
   requirements as well as minimum computational complexity,
3. procedures for the mapping of algorithms to special purpose hardware systems, and
4. procedures for the high level design of digital systems.

The course emphasizes the design of special purpose and application specific computer
systems for applications that require high performance such as digital signal processing,
communications and image processing.

TEXT AND REFERENCES
On line course notes will replace the primary text for this course. Additional references
include:
2. David R. Smith and Paul D. Franzon, Verilog Styles for Synthesis of Digital Systems,
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The course requirements are:
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2. a final exam,
3. homework assignments including some that require writing computer programs to
   model and simulate hardware designs.

The computer work will involve algorithm development, system design and simulation. We
will discuss the use of Matlab, Verilog and the C language for simulations in the class. The
University computing system will be used for all required computer simulations, etc. Other
classes such as ECE 406 and ECE 520 use Verilog and lockers for these courses have helpful
hints on its use.

A PC or any workstation may be used instead of the Eos computing system with appropriate
software as follows:
1. Verilog (Simucad provides a free download demo version of the Silos Verilog simulator
   Verilog HDL Demo Software are 200 gates and 350 lines of behavioral code.)
2. Matlab (The student version of Matlab with the Signal Processing Tool Box and
   Simulink is adequate)

GRADING POLICY
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For more information on NC State's policy on working with students with disabilities, please see
http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html

ACADEMIC INTEGRITY
All the provisions of the code of student conduct apply to this course as appropriate. See
http://www2.ncsu.edu/prr/student_services/student_conduct/POL445.00.1.htm